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## (54) Mould, pattern of nano wires, multiplexer/demultiplexer and method of making same

(57) A mould (110) with a protruding pattern (110a, 110b) is provided that is pressed into a thin polymer film (112, 312) via an imprinting process. Controlled connections between nanowires (118, 318) and microwires (116, 316) and other lithographically-made elements of electronic circuitry are provided. An imprint stamp is configured to form arrays of approximately parallel nanowires which have (1) micro dimensions in the X direction, (2) nano dimensions and nano spacing in the Y direction, and three or more distinct heights (12a, 12b, 12c) in the Z direction. The stamp thus formed can be used to connect specific individual nanowires (118, 318) to specific microscopic regions of microscopic wires (116, 316) or pads. The protruding pattern (110a, 110b) in the mould (110) creates recesses (112a, 112b) in the thin polymer film (112, 312), so the polymer layer acquires the reverse of the pattern on the mould (110). After the mould (110) is removed, the film is processed such that the polymer pattern can be transferred on a metal/semiconductor pattern on the substrate (114, 314).

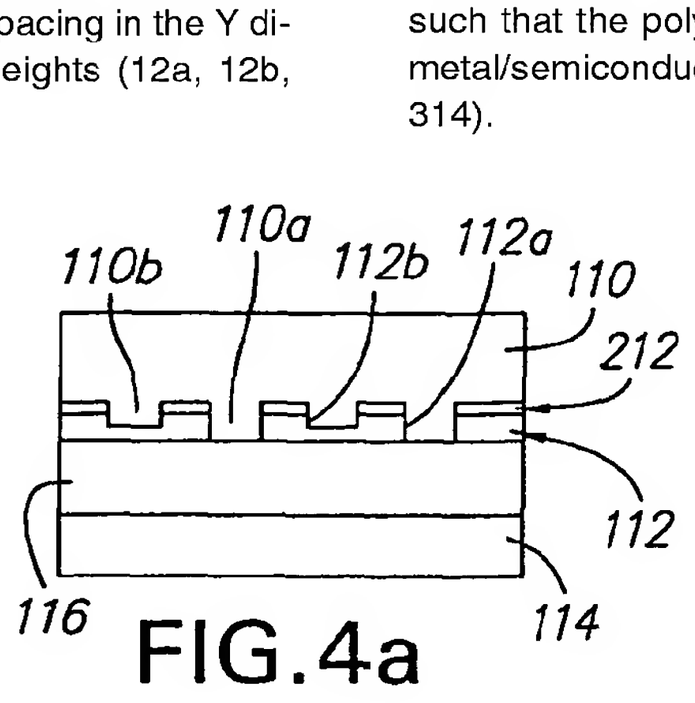


FIG.4a

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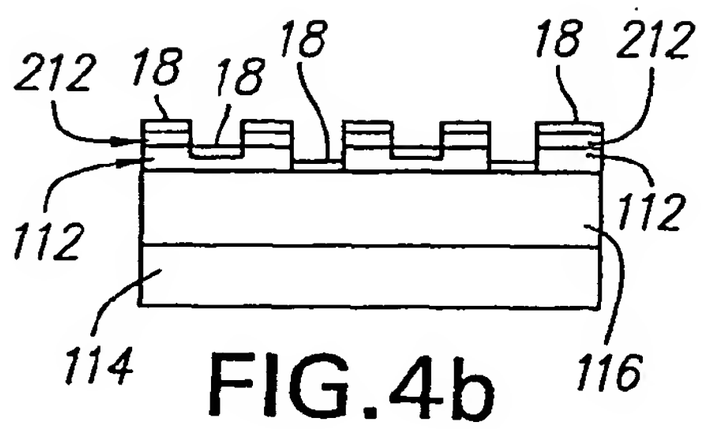

212
18
18
18
18
212
112
112
114
116

FIG.4b

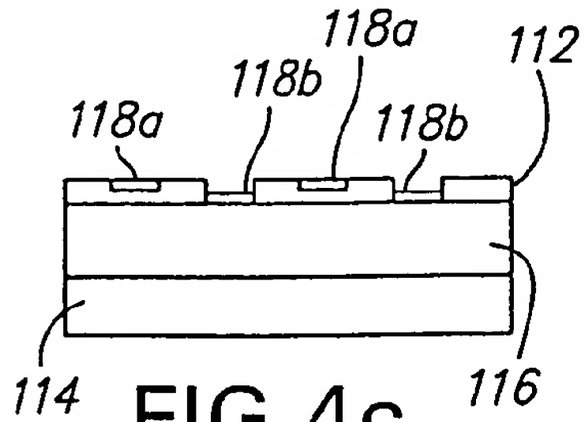

118a
118b
118a
118b
112
114
116

FIG.4c

## Description

**[0001]** The present invention is related generally to nanometer-size electronic circuits, including molecular electronics, and, more particularly, to providing an interface between nanowires that comprise nanometer-size electronic circuits and microwires that comprise micron-size electronic circuits for efficient input/output of electrical signals.

**[0002]** The fabrication of nanometer-size electronic circuits with a high density of elements, high operational speed, and low manufacturing cost promises wide applications in future electronic devices. However, a major problem for nanoelectronics is to develop methods to fabricate an interface between nanowires and external microwires. Such interfaces are needed to efficiently input/output electrical signals from the external circuitry into the nanowires, selectively supply and distribute power, and provide internal interconnects between the nanowires. In conventional microelectronics, these problems are solved by means of selective interconnections of the electronic elements. An example is the multiplexer/demultiplexer interface shown in FIG. 1 and described in detail below. At the nanoscale, such interfaces require selective connection or disconnection between the nanowire and microwire at each cross point. As a result, the feature size along the microwire has to be comparable with the width of the nanowire and with the spacing between them, so it has to be of nanoscale itself. This is impossible to achieve by conventional photolithographic means with current mechanical accuracy for positioning one set of features over another.

**[0003]** One example of such interconnections between nanowires and microwires is disclosed in U.S. Patent 6,256,767, entitled "Demultiplexer for a Molecular Wire Crossbar Network (MWCN Demux)", issued to Philip J. Kuekes et al on July 3, 2001, and assigned to the same assignee as the present application, the contents of which are incorporated herein by reference. That patent discloses a randomly patterned demultiplexer for a two-dimensional array of a plurality of nanometer-scale switches (a molecular wire crossbar network), employing a bistable molecule as a connector species connecting pairs of crossed wires at each junction in the crossbar network. The present application is an improvement there-over in that, as disclosed and claimed herein, a method of fabricating a pre-determined pattern of nanowire-microwire connections is provided, thereby reducing the number of microwires required and reducing the area occupied by the multiplexer/demultiplexer.

**[0004]** According to an aspect of the present invention, there is provided a mould as specified in claim 1.

**[0005]** According to another aspect of the present invention, there is provided a method of making a mould as specified in claim 4.

**[0006]** According to another aspect of the present invention, there is provided a pattern of nanowires as specified in claim 6.

**[0007]** According to another aspect of the present invention, there is provided a method of making a pattern of nanowires as specified in claim 7.

**[0008]** According to another aspect of the present invention, there is provided a multiplexer/demultiplexer as specified in claim 12 or 13.

**[0009]** According to another aspect of the present invention, there is provided a method of making a multiplexer/demultiplexer as specified in claim 17 or 19.

**[0010]** The preferred embodiments disclosed herein can provide a system for making arbitrary connections from specific microwires to specific nanowires.

**[0011]** In accordance with the embodiments disclosed herein, a mould with a protruding pattern is pressed into a thin polymer film via an imprinting process.

**[0012]** Controlled connections between nanowires and microwires and other lithographically-made elements of electronic circuitry are provided. An imprint stamp is configured to form arrays of approximately parallel nanowires that have (1) micro dimensions (lengths) in the X direction, (2) nano dimensions (widths) and nano spacing in the Y direction, and three or more distinct heights in the Z direction at the nanometer scale. The stamp thus formed can be used to create a multilevel imprint in a polymer layer (or multi-layer) that will enable the connection of specific individual nanowires to specific microscopic regions of microscopic wires or pads.

**[0013]** The protruding pattern in the mould creates a recess in the thin polymer film, so the polymer layer acquires the reverse of the pattern on the mould. After the mould is removed, the film is processed such that the polymer in the recess area is removed, thereby exposing the underlying substrate. By further processing, the polymer pattern can be transferred into a metal/semiconductor pattern on the substrate, either by etching recesses into an underlying conductive film with the patterned polymer as a mask or by evaporating conductive material over the patterned polymer and removing anything not contacting the underlying substrate by lifting off the remaining polymer.

**[0014]** The controlled connections can be used, for example, (1) to make a demultiplexer, (2) to connect a nanowire array to microscopic wires or pads for the general input/output of signals or to deliver power at distinct voltages to specific nanowires, (3) to connect multiple nanowires to a single microwire to use that microwire as a bus for digital signals, (4) to connect nanowires to a two-dimensional array of micro scale pads which are formed as vias by a conventional lithographic process, or (5) to selectively connect nanowires that belong to different layers of nanowires.

**[0015]** The preferred embodiments can solve the problem of selective connectivity between the external circuitry and nanowires. They can also allow simultaneous fabrication of nanowires and multiplexers/demultiplexers. They can also provide a technique for fabricat-

ing deterministic nanoscale integrated circuits, i.e., without recourse to random connections.

**[0016]** Embodiments of the present invention are described below, by way of example only, with reference to the accompanying drawings in which:

FIG. 1 is a schematic diagram of an example of a basic resistor-logic or diode-logic or transistor-logic demultiplexer circuit, in which three pairs of (horizontal) address wires that are interfaced to conventional circuitry are used to select one of eight nanowires (vertical); the round solid circles represent electrical (physical) contacts between the horizontal and vertical wires, and where there is no solid circle, there is no electrical or physical connection between the wires - they are separated by an insulating layer;

FIG. 2 is a perspective view, depicting a prior art imprinting process for which the features on the mould have only two levels;

FIGS. 3a-3b are perspective views, depicting a prior art imprinting and etch process for which the features on the mould have only two levels;

FIGS. 4a-4c are each a cross-sectional view, depicting one embodiment of the sequence of steps in fabricating a multiplexer-demultiplexer interface using a tri-level mould;

FIGS. 5a-5b are each a cross-sectional view, taken normal to the view of FIGS. 3a-3c, depicting the resulting configurations resulting in electrical noncontact, i.e., there is a thin insulating film between upper and lower wires (FIG. 5a) and electrical contact, i.e., there is a direct physical contact between the upper and lower wires (FIG. 5b);

FIGS. 6a-6e illustrate another embodiment of the formation of electrically connected sets of nanowires and microwires, involving an etch process;

FIG. 7 depicts an example of a nanowire-microwire connection in accordance with embodiments taught herein, for which a nanowire makes physical contact with certain larger wires, but does not make physical or electrical contact with other larger wires because of the insulating barrier between the two;

FIG. 8 illustrates a conventional demultiplexing scheme, employed in the practice of the various embodiments taught herein, where the dark areas indicate that there is physical and electrical contact between an upper and lower wire, and the absence of a dark area represents that the upper and lower wires are not in physical and electrical contact, i.e., they are separated by an insulating barrier;

FIG. 9 shows an embodiment depicting electrical connection of several nanowires to a microwire (represented by dark areas on center microwire) that does not extend outside the nanowire area of the nanowire array, which may be used for connecting a specific set of nanowires to each other or to some circuit element that lies under the plane of the larger wires (e.g., the wire shown represents a via from a lower layer of circuitry);

FIG. 10 illustrates selective connections between nanowires and microsized vias on two different levels; the nanowires are closest to the viewer, where a first microwire is below the nanowires and has a via that is used in this case to connect just one nanowire, and a second microwire is below the first microwire and has a via that is used to connect to a different nanowire;

FIG. 10a is an enlargement of a portion of FIG. 10, depicting electrical contact between a nanowire and a microwire;

FIG. 11 illustrates two interconnects between different layers of nanowires, with certain vias allowing connection between one nanowire in each layer, and other vias allowing connection between two different nanowires in the layers;

FIG. 12 is a perspective view, showing electrical contact of selected portions of nanowires to selected portions of microwires, with a switchable molecular film on the microwires;

FIG. 13 illustrates a set of curved nanowires selectively connected to a set of irregularly shaped microwires or macropads;

FIGS. 14a-14g illustrate a process for fabricating a three-level mould useful in the practice of the embodiments taught herein; and

FIGS. 15a-15c illustrate a superlattice-with-nanoparticles process for fabricating a three-level mould useful in the practice of the embodiments taught herein.

Definitions:

**[0017]** The term "micron-scale dimensions" refers to dimensions that range from 1 micrometer to a few micrometers in size.

**[0018]** The term "sub-micron scale dimensions" refers to dimensions that range from 1 micrometer down to 0.04 micrometers.

**[0019]** The term "nanometer scale dimensions" refers to dimensions that range from 0.1 nanometers to 40 nanometers (0.04 micrometers).

**[0020]** The term "microwire" refers to a wire with micron-scale or sub-micron scale width or diameter.

**[0021]** The term "nanowire" refers to a wire with nanometer-scale width or diameter.

**[0022]** The term "electrical contact" refers to an electrical connection between any two wires where that connection has 2-terminal ohmic or diode electrical character or 3-terminal transistor electrical character.

Imprinting Process:

**[0023]** Turning first to FIG. 1, a schematic diagram of a basic demultiplexer circuit is shown. Eight nanowires (marked as 1-8) can be addressed by six communica-

tion wires, which are controlled pairwise by three logical inputs (marked as A, B, and C). The upper wire of each pair is biased with the voltage that represents the compliment of the input value (1 or 0), and the lower wire is biased with the voltage that represents the input value. Any combination of 0s and 1 s on A, B, and C, uniquely addresses only one nanowire out of eight. For example, 1 on A, 1 on B, and 0 on C, will address the nanowire 6, and so on. In general, with such kind of multiplexer/demultiplexer circuits, 2n external microwires can interface with 2n nanowires; in other words, adding one pair of communication wires in the demultiplexer doubles the number of nanowires that can be addressed. However, as mentioned above, the feature size along the communication wires (A, B, C) has to be comparable with the width of the nanowires and with the spacing between them, so it has to be of nanoscale itself, and this is presently impossible to achieve by conventional photolithographic means.

**[0024]** Imprinting lithography is an effective, low-cost method to fabricate nanoscale circuits; see, e.g., U.S. Patent 5,772,905, entitled "Nanoimprint Lithography", issued on June 30, 1998, to S.Y Chou. FIG. 2 illustrates the imprinting process for a lift-off implementation, wherein a mould 10 with a protruding pattern 10a has been pressed into a thin polymer film 12. The polymer film 12 is supported on a substrate 14.

**[0025]** The protruding pattern 10a in the mould 10 creates a corresponding recess 12a in the thin polymer film 12 during pressing, so the polymer film acquires the reverse of the pattern on the mould. After the mould 10 is removed, the polymer film 12 is processed such that any polymer remaining in the recess area 12a is removed (in the case that the protrusions 10a did not fully contact the surface of the substrate 14), exposing corresponding portions of the underlying substrate 14. In the lift-off implementation here illustrated, a conductive thin film is deposited from the top direction, and the polymer portion 12b is dissolved in solvent, thereby removing the conductor deposited on the top of the polymer along with the polymer. Thus, only the conductor remaining in the recesses 12a will remain, thereby creating the desired pattern, e.g., conducting wires (not shown).

**[0026]** FIGS. 3a-3b illustrates the prior art imprinting process in the case of an etch implementation. As shown in FIG. 3a, substrate 14 supports a thin conductive film 18 and a thin polymer film 12. The mould 10 has been pressed into the polymer 12 to create recesses 12a, exposing portions of the conductive film 18. A subsequent etch process removes all exposed portions of the conductive film 18. Only portions of the film 18 still protected by the patterned polymer 12 remain. The patterned polymer 12 can then be removed, e.g., dissolved in solvent, to leave the patterned conducting wires 18 in FIG. 3b.

**[0027]** In accordance with the present embodiments disclosed herein, a method for fabricating multiplexer/demultiplexerlinterconnect interfaces is provided, using imprinting lithography technology. It is scalable down to the nanometer size and allows a simultaneous fabrication of the nanowire and multiplexer sections of the device.

**[0028]** A mould with a protruding pattern is pressed into a thin polymer film via an imprinting process. Controlled connections between nanowires and microwires and other lithographically-made elements of electronic circuitry are provided. The imprint stamp, or mould, is configured to form arrays of approximately parallel nanowires which have (1) micro dimensions in the X direction, (2) nano dimensions and nano spacing in the Y direction, and three or more distinct heights in the Z direction. The stamp thus formed can be used to create a multilevel imprint in a polymer layer (or multi-layer) that will enable the connection of specific individual nanowires to specific microscopic regions of microscopic wires or pads.

**[0029]** Whereas the protruding, wire-like regions 10a on an imprinting mould 10 are of the same height in the prior art mould shown in FIG. 2, on the multilevel imprint mould, variable heights are provided in the multiplexer/demultiplexer area, as shown in FIGS. 4a and 7. Specifically with reference to FIG. 4a, a higher region 110a of the mould 110 will make a correspondingly deeper recession 112a in the polymer thin films 112, 212. Technologically, it is better to use double-layer polymer thin films 112, 212 in some cases.

**[0030]** One example of the formation of wires is now described with reference to FIGS. 4a-4b, involving a lift-off process. Other examples of the formation of wires are described below.

**[0031]** Shown in FIG. 4a is a substrate 114 supporting a communication microwire 116. It is to this communication wire 116 that electrical contact will or will not be made in fabricating a multiplexer/demultiplexer such as shown in FIG. 1. The protrusions 110a and 110b can have heights ranging from 1 to 500 nm, with protrusion 110a about 0.1 to 100 nm higher than protrusion 110b.

**[0032]** In actuality, a plurality of communication microwires 116 is formed on the substrate 114, generally aligned parallel to each other. The formation of such communication microwires 116 is conventional and does not form a part of this invention. The communication wires 116 typically comprise a metal, such as aluminium, platinum, or a metallic silicide. Alternatively, single crystal or polycrystalline silicon, doped to an appropriate level, may be used as the communication wires 116.

**[0033]** After the mould 110 is removed, the polymer in the deeper recess areas is removed, thereby exposing the underlying communication microwire 116. However, the polymer in the shallower recess areas will not be completely removed, therefore the underlying communication wire 116 will not be exposed in those areas.

**[0034]** Next, metal 18 is blanket-deposited on top of the entire structure (FIG. 4b). Examples of suitable metals include those metals, metallic silicides, and silicon

(doped) listed above. During the following lift-off, polymer thin film 212 is dissolved in a solvent, but polymer thin film 112 remains intact. (This process relies on specifically selected pair of polymers so that the solvent only dissolves polymer 212 but not 112; the selection of such pairs of polymers and the appropriate solvent is well-known. For example, polymer thin film 212 can be PMMA (poly(methyl methacrylate)), which can be dissolved in acetone solvent; polymer thin film 112 can be polyimide, which does not dissolve in acetone.)

**[0035]** After the lift-off, the nanowires are fabricated in the circuits (not shown). In the multiplexer/demultiplexer area, the nanowires 118a in the shallower recess area do not make electrical contact with the communication wire 116 (see FIGS. 4c and 5a), while the nanowires 118b in the deeper recess area do make electrical contact with the communication wire 116 (FIGS. 4c and 5b). The nanowire circuit and multiplexer/demultiplexer are defined simultaneously.

**[0036]** Essentially, in the lift-off process, the required substrate consists of a relatively thick insulating material 114 topped by a deterministic array of large microwires 116. The process consists of imprinting a multi-level mould 110 into a multiple layer soft lithographic resist 112, 212 to create multi-level relief. Material de-posited on top of the resist layer follows the relief pattern to form nanowires 118. Excess material between the nanowires on the topmost resist surface is removed by dissolution of the supporting resist layer immediately below. Electrical contact between the nanowires 118 and microwires 116 occurs at all extreme projecting surfaces 110a of the imprint mould.

**[0037]** The relief of the nanowires 118a, 118b formed is related to the height of the protrusions 110, 110b, and is in the range of 1 to 500 nm. The nanowires 118a, 118b have a thickness of about 1 to 1000 nm.

**[0038]** The nanowires 118a, 118b are formed generally parallel to each other, and cross over the communication microwires 116 at a non-zero angle, typically orthogonal thereto, as shown in FIG 1. It will be appreciated by those skilled in this art that the dots at the various intersections in FIG. 1 are equivalent to those areas in which nanowires 118b make electrical contact with the communication microwires 116 and that the intersections not having dots in FIG. 1 are equivalent to those areas in which nanowires 118a do not make electrical contact with the communication microwires 116.

**[0039]** A second example of the formation of wires is now described with reference to FIGS. 6a-6e, involving an etch process. The required substrate consists of a thick insulating material 314 topped by a thin layer of device material 318, metal or semiconductor. The process consists of imprinting a multilevel mould 310 with recesses of a first depth 310b and a second depth 310a into a single or multiple layer soft lithographic resist 312 to create wire-like polymer protrusions with multi-level relief, portions of each protrusion having either a first height 312b or a second height 312a (FIGS. 6a-6b). Single or multiple etch steps, either dry, possibly reactive, ion etches or wet chemical etches then transfer the multi-level relief from the resist down into the thin device material layer 318 (FIG. 6c). At this stage the continuous device material layer 318 has been patterned into nanowires with multi-level thicknesses or heights 318b and 318a above the thick insulating substrate. Planarization with insulating material 319 at the level of the topmost de-vice material 318c then results in a flat surface with isolated exposed portions 318c of the mostly buried nanowires (FIG. 6d). These isolated exposed portions 318c are then contacted by large scale microwires 316 deposited and patterned by conventional lithographic techniques (FIG. 6e). Insulating material 319 can be formed by several methods including vapor phase regrowth or electrochemical regrowth of the insulating substrate 314, or blanket deposition of similar or different insulating material. Planarization can be achieved by chemical and/or mechanical polishing.

**[0040]** The present teachings provide a means for fabricating a multiplexer/demultiplexer/interconnect by imprinting, simplifying the manufacturing processes, and allowing the multiplexer/demultiplexer/interconnect and nano-circuits to be fabricated simultaneously. Therefore, it solves the connection/communication problem for nanoscale circuits including molecular electronic circuits.

Applications

**[0041]** The teachings herein provide a general method of making controlled connections between nanowires and microwires and other lithographically-made elements of electronic circuitry. The various embodiments create an imprint stamp to make systems of approximately parallel nanowires, which have micro dimensions in the X direction, nano dimensions and nano spacing in the Y direction, and three or more distinct heights in the Z direction. This stamp can be used to connect specific individual nanowires to specific microscopic regions of microscopic wires or pads; see FIG. 7.

**[0042]** As shown in FIG. 7, a three-level mould stamped into polymer 10 creates a three-dimensional landscape, comprising a first level 12a exposed through windows 15 that extend to the top surface of communication wires 116a, 116b, a second level 12b that defines the continuous nanowires 118a, 118b, and a third level 12c. Each groove at level 12b has its own set of windows 15 that expose microwires 116a-116c underneath the stamped polymer 10. After deposition of metal and liftoff (not shown), nanowires 118 are formed at level 12b, including following the contours at that level and into windows 15 that may be present. Nanowires 118 connect to microwires 116 only through windows 15 and make contact at locations 20. In this particular embodiment depicted in FIG. 7, nanowire 118b connects to microwires 116a and 116b but does not connect to microwire 116c. (The connection between microwire 116b and na-

nowire 118a is denoted 22, since it is hidden in the view shown in FIG. 7.)

**[0043]** An X-Y-Z coordinate system is depicted in conjunction with FIG. 7, wherein the mould, or imprint stamp, is configured to form arrays of approximately parallel nano-wires 118 which have (1) micro dimensions in the X direction, (2) nano dimensions and nano spacing in the Y direction, and three or more distinct heights in the Z direction (three such heights are shown in FIG. 7).

(1) In one embodiment, the connection depicted in FIG. 7 may be used to make a demultiplexer; see FIG. 8. As shown in FIG. 8, each pair of communication wires 216a, 216b, 216c, and 216d, each on the order of micrometer size, divide a set of sixteen nanowires 218 in half, but in its own way, as illustrated, for example, by black areas 20 under the nanowires 218 where they electrically contact the communication wires 216. Open circles denote the logical operation NOT. As a result, any combination of 0s and 1 s sent to 216a, 216b, 216c, and 216d selects one and only one nanowire 218. An external signal 26 is sent through all nanowires 218, but only the selected wire carries the signal to the nanowire circuit (not shown but denoted by arrow 28).

The nanowire circuit could be a nanowire-nanowire cross-bar structure, such as disclosed in, for example, U.S. Patent 6,128,214, entitled "Molecular Wire Crossbar Memory", issued on October 3, 2000, to Philip J. Kuekes et al and assigned to the same assignee as the present application; the contents of U.S. Patent 6,128,214 are incorporated herein by reference. Every intersection is a memory element (memory circuit), or a logic element (computer logic circuit). Accordingly, every nanowire circuit has to have at least two demultiplexers, one for X and another for Y arrays of nanowires. For the demultiplexer shown in FIG. 8, the microscopic wires 216 would be semiconductor (doped) or metal; the nanowires 218 would be metal or semiconductor. Electrical contact between the microwires and nanowires could have ohmic, diode or transistor character, with diode and transistor character most desirable for demultiplexer circuits.

The nanowire circuit could be a nanowire-nanowire crossbar structure, where every intersection is a nano-scale sensor or actuator element.

The nanowire circuit could consist of only one set of approximately parallel nanowires, possibly coated with chemical or biological functional groups, each nanowire acting as a sensor or actuator.

(2) In another embodiment, the connection depicted in FIG. 7 may also be used to connect a nanowire array to microscopic wires or pads for general input/output of signals or to deliver power at distinct voltages to specific nanowires (not shown).

(3) In yet another embodiment, multiple nanowires 318 may be connected to a single microwire 316b (and not to other microwires 316a, 316c) to use that microwire as a bus 30 for common signals; see FIG. 9. A short microwire 316b connects to selected nanowires 318, as illustrated by the black areas 20 under the nanowires where they electrically contact the short microwire.

(4) In still another embodiment, nanowires 418 may be connected to a two-dimensional array of micro scale pads 416 which are formed as vias by a conventional lithographic process; see FIGS. 10 and 10a. This embodiment allows high-density connections to multiple layers of microwires 416a, 416b. Contact 20 is made between nanowires 418 and micro scale pads, or vias, 416, because nano-contact is at multiple levels. Microscopic vias 416 and microscopic wires, or conductive paths, 516 are made by conventional lithography. Microscopic vias 416a, 416b come out close enough to make electrical contact 20 with nanoscopic wires 418. Microscopic via 416b extends to a first layer of conductors 516b, while microscopic via 416a extends even deeper to a second layer of conductors 516a. In a multi-layer circuit, there could be a plurality of such conductor layers 516, connected to nanoscopic wires 418 by microscale vias 416. This is a mechanism for connecting nanowires arbitrarily deep through vias.

One issue is that microscopic conductors 516a, 516b are quite large compared to nanowires 418. If it is desired to make electrical connections 20, one would be limited by the number of connections that could be made. The vias 416 permit more connections, using deeper layers. (As an aside, if one had a region full of circuits, say 2-dimensional, and wanted to connect to the external world, one could enclose the circuits in a line. The lines from each circuit have to "escape" the enclosure. The use of vias 416 permits escape on multiple layers.) For an area N, the number of circuits is N2, but only N lines allowed. But if there are N levels, then one can gain access to all circuits.

A second value is the specific connections allowed by contacts 20. FIG. 11, discussed next, is a generalization of the bus idea to multiple planes; FIG. 10 shows how to do this.

(5) In yet another embodiment, the basic approach depicted in FIG. 7 can be used to selectively connect nanowires 418 that belong to different layers of nanowires. This can be done by connecting the wires from two neighboring nanowire layers 36a, 36b to microwires 416a, 416b that are sandwiched in between. This provides a method to connect different nanowire layers together and create three-dimensional nanowire networks and circuits; see FIG. 11. Nanowires 418a in an array 36a are selectively connected to vias 416a. Nanowires 418b in an array 36b are selectively connected to vias 416b.

The vias 416a and 416b are connected between each other. As a result, specific connections of individual nanowires that belong to different levels is possible.

**[0044]** FIG. 11 is directed to connecting nanoscale arrays 36. A via 416 can be connected to a nanoarray 36, simply by considering the structure shown in FIG. 10 and connecting two such structures back-to-back. Nanowires 418a are in the foreground. Contact 20a is next closest. Via 416a is in front of via 416c. Via 416b is in the same plane as via 416a. Via 416b is in front of via 416d. The furthest plane contains nanowires 418b.

**[0045]** One can create a circuit using nanocrossbar technology and conventional microscale lithography. Shown here is one direction of crossbars, 418a. This gives conductivity between 418a and 418b, since the vias 416 are electrically conducting. Thus, one or more nanowires 418 can be connected to each other, in the same plane (which can also be done by the crossbar) or in different planes, using multiple distinct buses (416a-416c; 416b-416d). It is in principle possible to form a sandwich, stacking molecular crossbar circuits and permit them to talk with each other vertically, using an arbitrary, fixed pattern. This arrangement permits arbitrary routing, using electrical connections, without necessarily having direct physical connection, using microwires 416 in x and y directions. Electrical contact between the vias 416 and the nanowires 418 may have ohmic, diode or transistor character.

**[0046]** As will be appreciated by those skilled in this art, the teachings herein provide a method to fabricate complex connected integrated electronic circuits at the nanoscale.

Materials and Connections

**[0047]** The microwires and nanowires described herein may be metallic, semiconductor, or insulating, depending on the material used for their fabrication. They may alternatively be organic or molecular conductors. Consequently, the electrical connection between nanowires and microwires may be of ohmic, diode or transistor character. Alternatively, the connection may be insulating, for example, a tunnel barrier or anti-fuse designed to break down at a particular applied field. The teachings herein provide a method to make selective connections to a particular type of wires. For example, some nanowires may be connected only to metallic microwires while other nanowires are connected to semiconductor microwires. Or, the same nanowire may be connected to one or more metallic microwires and, at the same time, to one or more semiconductor microwires.

**[0048]** Additionally, a molecular film may be placed between a microwire and a nanowire at the point of their contact. FIG. 12 depicts such an arrangement. Here, three microwires 116a-116c are shown, together with two nanowires 118a-118b. A molecular film 40, comprising a plurality of molecules 40a and formed on the surface of the microwires 116, is sandwiched by a nanowire 118, wherever it contacts a microwire 116. For example, nanowire 118a contacts the molecular film 40 on microwires 116b and 116c (but not on microwire 116a), whereas nanowire 118b contacts the molecular film 40 on microwires 116a and 116b (but not on microwire 116c).

**[0049]** The molecules 40a in the molecular film 40 may be passive or active electronic elements. As passive elements, they may facilitate a better electrical contact between the nanowire 118 and the microwire 116, or enhance the rectifying function or transistor function of the connection. As active elements, they may be multiple-state switches or transistors.

**[0050]** Similarly to molecules, other substances may be placed between nanowires 118 and microwires 116 in their contact regions 20. These may be single or multiple layers of metal, insulator, semiconductor, polymer, or nanoparticles. These may also be alloys, mixtures of nanoparticles of different kinds, as well as more complex composites.

3. Geometries

**[0051]** The present teachings disclose a fabrication sequence in which the microwires 116 are fabricated first and then nanowires 118 are imprinted and fabricated on top thereof. However, this sequence may be reversed. That is, nanowires 118 are imprinted first and then microwires 116 are fabricated on top of the nanowires.

Further, microwires 116 may be placed inside as well as outside the footprint of the nanowire arrays 36.

**[0052]** Finally, according to the teachings of the various embodiments herein, connections may be made from microscale features 116 not only to straight nanowires 118, but also to systems of curvilinear approximately parallel nanowires; see FIG. 13. A system of curved nanowires 718, fabricated by imprinting, makes selected electrical connection to various lithographically fabricated microwires 716, which may or may not be curved.

4. Fabrication Methods

**[0053]** In one embodiment, a lift-off process may be used, as described above.

**[0054]** In another embodiment, an etch process may be used, as described above.

**[0055]** In yet another embodiment, a pattern for location of pre-fabricated nanowires may be used. The required substrate consists of a thick insulating material. The process consists of imprinting a multi-level mould into a multiple layer soft lithographic resist to create multi-level relief. Trenches formed in the resist are then used to guide deposition and alignment of pre-fabricated nanowires, for example carbon nanotubes. These

nanowires 118 can contact microwires 116 below following the initial substrate preparation of the lift-off process, or can contact microwires above following the final steps of the etch process.

**[0056]** In a still further embodiment, a pattern for in-situ nanowire growth may be used. It is almost identical to the preceding pattern process, except that the relief trenches 112a, 112b formed in the resist 112 are then used to initiate in-situ growth of device material, for example silicon nanowires or carbon nanotubes. These nanowires can contact microwires below following the initial substrate preparation of the lift-off process, or can contact microwires above following the final steps of the etch process.

5. Mould Design

5a. Two-Level Molds

**[0057]** The prior art for two-level moulds is described in U.S. Patent No. 5,772,905, "Nanoimprint Lithography" by Stephen Y. Chou. That patent describes the process of creating a hard mould with two different feature heights and pressing that mould into a thin polymer film on top of a substrate. By controlling the temperature and pressure during the imprint process, an imprint is made into the polymer layer. This imprint can then be cleaned up by a light etching process, to remove excess polymer at the bottom of the imprint channels. The remaining polymer may then be used as an etch mask for further etching into the substrate to form channels, or it may be used as a deposition mask for metal or other deposited material.

5b. Three-Level Moulds

**[0058]** The present teachings are directed to the fabrication of a hard mould in which there are features at three different levels in the mould. When this mould is pressed into a substrate, it will leave an impression with three different heights-one at or very near the substrate surface, one at an intermediate height above the surface, and a third that is higher than the second. For the case in which the substrate is itself a thin metal film on an insulating substrate, etching this system with an appropriate anisotropic etch will result in a surface with two different wire heights. Furthermore, the height of a particular wire can alternate between two different heights if the thickness of the mould alternates.

5c. Four- (or More) Level Moulds

**[0059]** This principle of creating moulds with more than two levels can be extended to four or more level systems. Such a mould can lead to the formation of a surface that has wires with three or more thicknesses. Such a system may be useful for the creation of complex three dimensional circuits based on nanowires.

6. Mould Fabrication

**[0060]** There are many methods for creating multi-layer moulds, some of which are discussed here. Most utilize a combination of techniques - some type of process to create a large number of nanometer-width features that will be the template for nanowires in the finished device, coupled with some other type of serial process that can be used to modify the template to add more levels and increase the complexity, and thus the information content, of the pattern.

6a. Superlattices

**[0061]** Creating extremely long parallel lines with a pitch in the sub 100 nm length range is extremely challenging for any lithographic process. One way to create a mould for imprinting such lines is to grow a superlattice of two materials, such as Si and SiGe alloys or GaAs and AlGaAs alloys. Well known and highly controlled methods can be used to grow atomically precise thicknesses of the two materials. When the wafer is cleaved perpendicular to the growth plane and then etched to preferentially remove one of the materials, an imprint mould with a large number of precisely parallel lines of predetermined width and height can be formed. To create the third level of features, this mould can be subsequently modified using locally focused etching or deposition techniques, to either remove or add material and create arbitrary patterns that cross over the parallel lines of the super-lattice.

6b. Locally Focused Etching

**[0062]** A critical step in the process of the present invention is to fabricate a mould 110 with different protrusive heights 110a, 110b. One suitable method is to use a locally focused source, for example, a focused ion beam or a nano-scale scanning electrochemical probe, to etch the existing mould 110, for example, pre-fabricated using the superlattice method described above. After the nanowire mould 110 has been made, protrusions 110a can be selectively etched locally by the focused beam to produce protrusions 110b. An arbitrarily patterned multilevel mould can be created. The height change can be controlled by the etching conditions, e.g., by etching time. This focused etching method could also be used starting from a planar substrate to create the multi-level mould in its entirety.

6c. Locally focused deposition

**[0063]** Another suitable method comprises use of a locally focused source, for example a focused ion beam or a focused electron beam catalyzing chemical vapor deposition or a nano-scale scanning electrochemical probe, to selectively deposit material onto the existing mould 110. After the nanowire mould 110 has been

made, for example with uniform protrusions 110b, the focused beam can be used to deposit additional material locally onto protrusions 110b to create higher protrusions 110a. An arbitrarily patterned multi-level mould can be created, with the relief height controlled by the deposition conditions, e.g., deposition time. The focused deposition technique could also be used starting from a planar substrate to create the multi-level mould in its entirety.

6d. Locally focused chemical modification

**[0064]** Instead of directly etching or depositing material the locally focused source could be used to locally chemically modify the existing mould 110. Subsequent exposure to chemical deposition conditions can result in material depositing on the locally modified regions of the mould. Alternatively, chemical etch conditions could be used to result in removal of material from the locally modified regions of the mould. Both approaches can generate an arbitrarily patterned multi-level mould.

6e. Patterned Superlattices

**[0065]** Superlattices can be fabricated and subsequently patterned to create the multi-level mould as described above. Alternatively, patterning can be done during the superlattice fabrication. In this method, thin layers of two materials, "A" and "B", are grown on a substrate in alternative order. Material "A" etches in certain wet or dry chemical environments much slower than material "B". During deposition of material "A", certain areas of the layer are shadowed, leaving empty regions, which are then filled with material "B" during deposition of the next layer. These shad-owed regions do not have to be nano-scale. Therefore, their size and exact locations could be controlled by conventional photolithographic processes. The pattern of shadowed regions could be made different and unique to different layers of material "A".

**[0066]** After depositing all the layers, the superlattice is cut in half through the shadowed regions of material "A". Then the side of the superlattice is exposed to the etch which removes material "B" from between the layers of material "A", as well as from the shadowed regions inside the layers of material "A". Hence, a unique pattern of protruding regions of material "A" is exposed on the side edge of the superlattice. The side of the superlattice can then be used as a mould. In this method, the width of nanowires is controlled by the thickness of layers "A". Therefore, the method is capable of producing multiplexers deep into the nano-scale. A similar scheme is disclosed and claimed in U.S. Patent 6,294,450, using alternating layers of two dissimilar materials.

**[0067]** An example of how to form three layer moulds is illustrated with reference to FIGS. 14a-14g. As shown in FIG. 14a, a first layer 50a of nanoscopic thickness is provided with a first opening 52a therethrough. The layer 50a comprises a material having a first composition. The opening 52a has microscopic lateral dimensions.

**[0068]** The opening 52a is next filled with a material 54a having a second composition, as shown in FIG. 14b.

**[0069]** Next, as shown in FIG. 14c, a second layer 154 of material having the second composition is deposited on the first layer 50a. The second layer 154, like layer 50a, is also of nanoscopic thickness.

**[0070]** The process is continued by adding a third layer 50b of the first composition and forming a second opening 52b through that third layer, as shown in FIG. 14d. The second opening 52b is formed not over the first opening 52a, but laterally displaced from it. The third layer 50b, like the previous layers, is of nanoscopic thickness, while the opening 52b, like the opening 52a, has microscopic lateral dimensions.

**[0071]** As above, the opening 52b is filled with a material 54b having the second composition, as shown in FIG. 14e.

**[0072]** Next, the structure 210 is cut through the openings 52a, 52b along the line denoted 56, as shown in FIG. 14e, to produce the structure 210a shown in FIG. 14f, thereby exposing the interior of the structure 210, along with the material 54a, 54b in the openings 52a, 52b.

**[0073]** Finally, an etchant is selected that etches the second material faster than the first material, and the structure 210a is etched from the side, providing a suitable mould 210b having three levels, 12a, 12b, 12c, as shown in FIG. 14g.

6f. Superlattice with Nanoparticles

**[0074]** Alternatively, the patterned superlattice method of FIGS. 14a-g can be implemented with nano-scale particles. During fabrication of the superlattice, nanoparticles 55 are incorporated into the alternate layers 50, as indicated in FIG. 15a. The arrangement of nanoparticles in the plane 50 can be patterned deterministically, for example by lithographic or self-assembly methods. Cutting the super-lattice perpendicular to the alternating planes 50, 154 then produces an edge with exposed nanoparticles 55 (FIG. 15b). Etching of the layers 154 produces a two-level mould as described above. The nanoparticle material is also chosen so as to have different etch characteristics than the layer 50. Subsequent etching of either the layers 50 or the nanoparticles 55 produces multi-level relief on the protruding surfaces 12a, shown in FIG. 15c. The nanoparticles 55 either protrude from the protruding surfaces 12a or are recessed therein, depending on the relative etch rates of the nanoparticles and the protruding surfaces.

**[0075]** The arrangement of nanoparticles may instead be patterned randomly, in which case successful implementation of a multiplexer function is more difficult but still possible, as disclosed in U.S. Patent 6,256,767, entitled "Demultiplexer for a Molecular Wire Crossbar Net-

work (MWCN Demux)", issued to Philip J. Kuekes et al on July 3, 2001, and assigned to the same assignee as the present application, the contents of which are incorporated herein by reference.

6g. E-Beam Bilayer Resist

**[0076]** Another procedure for creating a three-layer mould is to deposit two different layers of electron beam resist on a substrate. Writing into this bilayer at one beam intensity will only expose the top layer of resist, while writing with a more intense beam current will expose both layers of resist. After developing and stripping the developed resist, one is left with a three layer system that can then be etched into the mould substrate by the appropriate anisotropic etch.

**[0077]** The method for making a multiplexer/demultiplexer in nanoscale circuits by an imprinting process is expected to find use in the fabrication of nanometer-size electronic circuits, including molecular and polymer electronic circuits.

**[0078]** The disclosures in United States patent application no. 10/453,329, from which this application claims priority, and in the abstract accompanying this application are incorporated herein by reference.

## Claims

1. A mould with a protruding pattern (110a, 110b) for fabricating approximately parallel nanowires (118a, 118b) which have (1) micro dimensions in the X direction, (2) nano dimensions and nano spacing in the Y direction, and at least three distinct heights (12a, 12b, 12c) in the Z direction.

2. A mould as in claim 1, for connecting specific individual nanowires (118, 318) to specific microscopic regions of microscopic wires (116, 316) or pads.

3. A mould as in claim 1, for (1) making a demultiplexer, (2) connecting a nanowire array (218) to microscopic wires (216a, 216b, 216c, 216d) or pads for the general input/output of signals or to deliver power at distinct volt-ages to specific nanowires, (3) for connecting multiple nanowires (318) to a single microwire (316b) to use that microwire (316b) as a bus for digital signals, (4) connecting nanowires (418) to a two-dimensional array of micro scale pads (416) which are formed as vias by a conventional lithographic process, or (5) selectively connecting nanowires (418a, 418b) that belong to different layers of nanowires.

4. A method of making a mould as in claim 1, 2 or 3, including the forming said protruding pattern in said mould (110) having said at least three different distinct heights (12a, 12b, 12c) in the Z direction.

5. A method as in claim 4, wherein said mould (110) is fabricated by focused ion beam deposition or etching, or by electron beam catalyzed chemical vapour deposition or etching, or by nano-scale scanning probe electrochemical deposition or etching, or from electron beam bi-layer lithographic resist, or by a combination of electron beam lithography, photolithography, and focused ion beam lithography, or by using a superlattice construction involving alternating layers of two materials having different solubilities in a solvent, including modifying the superlattice construction with deposition or etching using an ion beam or an electron beam or a nanoscale scanning probe or with electron beam lithography or with photolithography or any combination thereof.

6. A pattern of nanowires (118a, 118b) which have (1) micro dimensions in the X direction, (2) nano dimensions and nano spacing in the Y direction, and at least three distinct heights (12a, 12b, 12c) in the Z direction, produced by a mould as in claim 1, 2 or 3.

7. A method of fabricating said pattern of claim 6, including the steps of:

providing a polymer film (112) supported on a substrate (114, 314));
providing a mould (110) having at least three levels of protruding patterns (12a, 12b, 12c);
stamping said mould (110) into said polymer film (112) to create at least three levels therein; and
forming said nanowires (118) in each of said three levels.

8. A method as in claim 7, wherein said nanowires (118) are formed by a lift-off process including the steps of:

providing a substrate (114) including an insulating portion (114) and a layer of an array of microwires (116) thereon, with said polymer film (112) formed on said layer of microwires (116);
forming a lithographic resist (212) on said polymer film (112);
stamping said mould (110) into said polymer film (112) to form a multilevel relief, whereby portions (110a) of said protruding patterns penetrate to said layer of array of microwires (116), thereby exposing said layer, and whereby other portions (110b) of said protruding patterns penetrate below said lithographic resist (212) into said polymer film (112) thereby to expose portions of said polymer film (112), and whereby still other portions of said protruding patterns do not penetrate said lithographic resist (212);

blanket-depositing conductive material (18) on said exposed portions of said layer of array of microwires (116), on said exposed portions of said polymer film (112), and on said lithographic resist (212) not otherwise penetrated; and
dissolving portions of said resist (212) to remove conductive material thereon (18), leaving conductive material, including a set of said nanowires (118a) in contact with said exposed portions of said layer of array of nanowires (116) and at least one additional set of nanowires (118b) supported above said layer of array of microwires (116) by said polymer film (112) to form conductive traces.

**9.** A method as in claim 7, wherein said nanowires (118) are formed by an etch process including the steps of:

providing said substrate (314) including an insulating portion (314) and a conducting layer (318) thereon, with said polymer film (312) formed on said conducting layer (318);
stamping said mould (110) into said polymer film (312) to form a multilevel relief;
etching said polymer film (312) to transfer said multi-level relief in said lithographic resist (312) down into said conducting layer (318) to form nanowires (318a, 318b) with multi-level relief along their length;
planarizing with insulating material (319) at the topmost conducting layer to leave said topmost conducting layer exposed (318b); and
electrically contacting said exposed topmost layer (318b) with patterned microwires (316).

**10.** A method as in claim 7, wherein said nanowires (118) are pre-fabricated and are located in pre-determined locations as follows:

providing said substrate (114) including an insulating material;
forming a polymer film (112) on said insulating substrate (114);
stamping said mould (110) into said polymer (112) film to form a multilevel relief, including trenches (112a, 112b);
using said trenches (112a, 112b) formed in said polymer film (112) to guide deposition and alignment of said pre-fabricated nanowires (118);

(1) whereby in the case where microwires (116) are deposited on said insulating substrate (114) prior to forming said polymer film (112) thereon, windows in the polymer film (112) opened by the furtherest protruding surface of the mould relief expose portions of said microwires (116) for electrical contact by said pre-fabricated nanowires (118), or
(2) whereby in the case where microwires (116) are deposited on top of said nanowires (118), then an etch process is first implemented to transfer said multilevel relief into said substrate (114) and said deposited nanowires (118) then replicate said multi-level relief, and planarization with an insulating material (319) then leaves deterministic exposed portions of said nanowires (118), and said microwires (116) are patterned and formed on portions of said pre-fabricated nanowires (118), making electrical contact only to said exposed portions.

**11.** A method as in claim 7, wherein said pattern permits connecting specific individual nanowires (118) to specific microscopic regions of microscopic wires (116) or pads.

**12.** A multiplexer/demultiplexer for nanoscale circuits including:

(a) a substrate (114) provided with a major surface;
(b) a plurality of bottom communication wires (116) formed on said major surface;
(c) a polymeric film (112) provided with a plurality of first recesses (112a) and a plurality of second recesses (112b), wherein said first recesses (112a) are deeper than said second recesses (112b) and wherein said first recesses (112a) expose portions on one or more of said bottom communication wires (116); and
(d) a metal layer (18) formed in the bottom of both said first recesses (112a) and said second recesses (112b) that forms wires (118) that cross over said bottom communication wires (116) at a non-zero angle, whereby said wires (118b) in said second recesses (112b) do not make electrical contact with said bottom communication wire (116) and whereby said wires (118a) in said first recesses (112a) do make electrical contact (20) with said bottom communication wire (116).

**13.** A multiplexer/demultiplexer for nanoscale circuits including:

(a) a substrate (314) provided with a major surface;
(b) a plurality of bottom nanowires (318a, 318b) formed on said major surface, with multi-level relief along the length of the nanowires (318a. 318b);

(c) an insulating film (319) formed on said bottom nanowires (318a, 318b), covering all of said nanowires (318a, 318b) except those portions comprising the uppermost relief level;
(d) a plurality of upper communication wires (316) that cross over said bottom nanowires (318) at a non-zero angle, whereby said communication wires (316) make electrical contact with said nanowires (318b) only at said uppermost relief level portions of said nanowires (318b) that remain uncovered by said insulating film (319).

**14.** A multiplexer/demultiplexer as in claim 12 or 13, wherein said plurality of nanowires (118, 318) are generally parallel to each other.

**15.** A multiplexer/demultiplexer as in claim 12 or 13, wherein said plurality of communication wires (116, 316) are generally parallel to each other.

**16.** A multiplexer/demultiplexer as in any one of claims 12 to 15, wherein said nanowires (118, 318) have a height in a range of about 1 to 1000 nm and a width in a range of about 1 to 1000 nm.

**17.** A method of making a multiplexer/demultiplexer as in claim 12, by an imprinting and lift-off process, said method including the steps of:

providing a substrate (114) with at least one bottom communication wire (116) on a major surface thereof;
forming a first polymer layer (112) on said major surface of said substrate (114), said first polymer layer (112) having a first thickness;
forming a second polymer layer (212) on said first polymer layer (112), said second polymer layer (212) having a second thickness and capable of dissolving at a faster rate in a solvent than said first polymer (112);
providing a mould (110) having a plurality of wire-like protrusions (110a, 110b), portions of each protrusion having either a first height or a second height, wherein said first height is greater than said second height, wherein said first height is equal to the total of said first and second thickness and wherein said second height is less than said second thickness;
impressing said wire-like protrusions (110a, 110b) of said mould (110) into said first and second polymer layers (112, 212) such that said first height penetrates said first and second polymers to said bottom communication wire (116) to thereby create a plurality of shallow recesses (112b) and a plurality of deep recesses (112a);
blanket-depositing a metal layer (18) on said second polymer and in said shallow and deep recesses;
removing said second polymer (212) and said metal layer (18) thereon, thereby leaving metal (118b) in said shallow recesses (112b) that does not make electrical contact said bottom communication wire (116) and leaving metal (118a) in said deep recesses (112a) that does make electrical contact with said bottom communication wire (116).

**18.** A method as in claim 17, wherein said mould (110) is fabricated by using a focused ion beam to selectively etch said protrusions (110a, 110b) of said first and second heights.

**19.** A method of making a multiplexer/demultiplexer as in claim 13, by an imprinting and etch process, said method including the steps of:

(a) providing a substrate (314) with a major surface;
(b) forming a conductive layer (318) on said major surface of said substrate (314);
(c) forming a polymer layer (312) on said conductive layer (318), said polymer layer (312) having a thickness;
(d) providing a mould (310) having a planar surface and a plurality of wire-like recesses, portions of each recess having either a first depth (310b) or a second depth (310a), wherein said first depth is greater than said second depth, wherein said first depth is equal or greater than said polymer thickness and wherein said second depth is less than said polymer thickness;
(e) impressing said mould (310) into said polymer layer (312) such that said planar surface penetrates said polymer (312) to said conductive layer (318) to thereby create a plurality of wire-like polymer protrusions with multi-level relief, portions of each protrusion having either a first height or a second height;
(f) transferring the multi-level relief of said imprinted polymer layer (312) into said conductive layer (318) by single or multiple etch processes, to form conductive wires (318a, 318b) with multi-level relief, portions of each wire have a first height or a second height, wherein said first height is greater than said second height;
(j) forming an insulating layer (319) on top of said conductive wires (318) by deposition or growth processes;
(k) planarizing said insulating layer (319) at the level of the topmost conductive wire portions of said first height, to leave a plurality of conductive wires (318) covered by said insulating layer (319) except exposed at those portions of said first height;
(l) forming a plurality of upper communication

wires (316) supported by said planarized insulating layer (319), that make electrical contact to said lower conductive wires (318a) only at those portions of said first height not covered by said insulating layer (319).

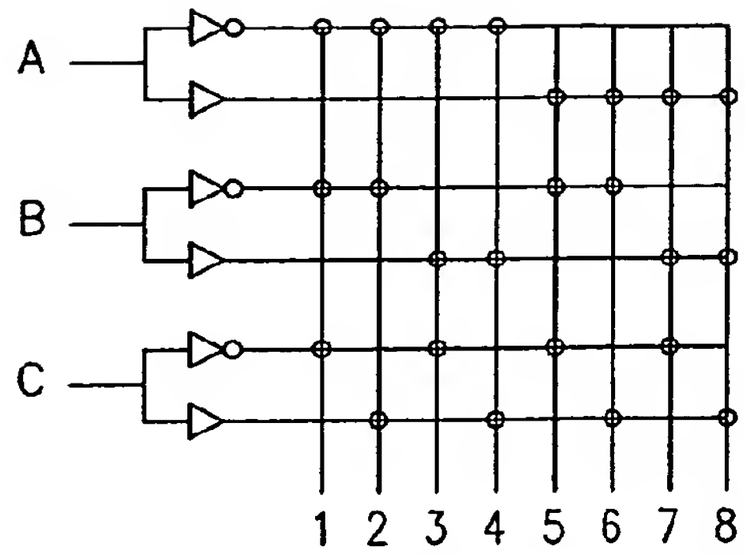



FIG.1
PRIOR ART

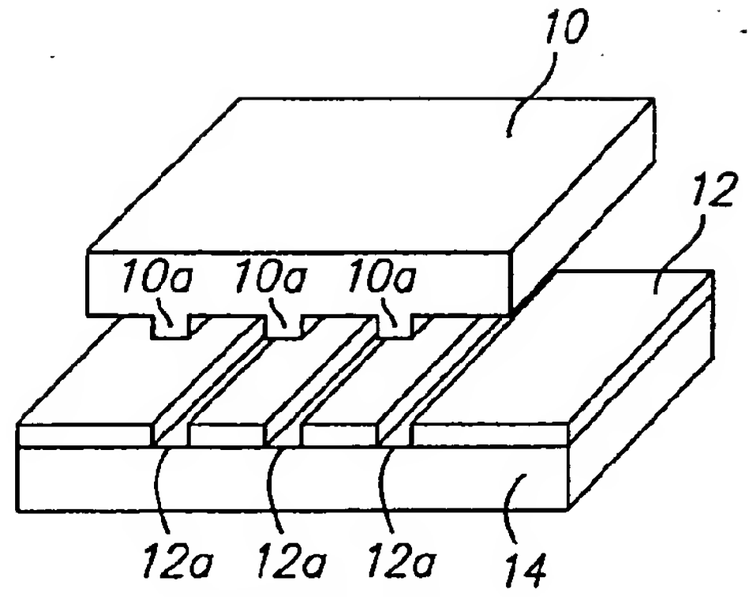



FIG.2
PRIOR ART

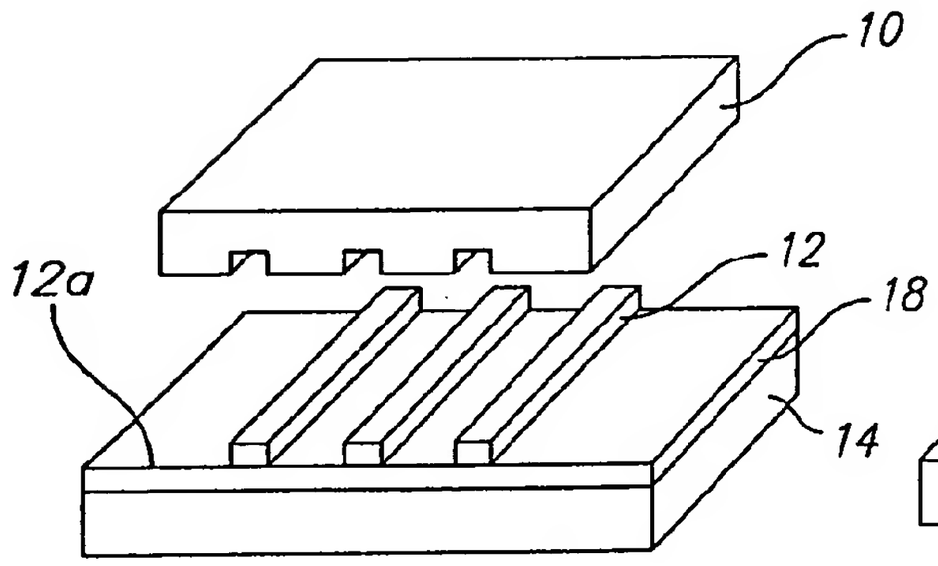



FIG.3a
PRIOR ART

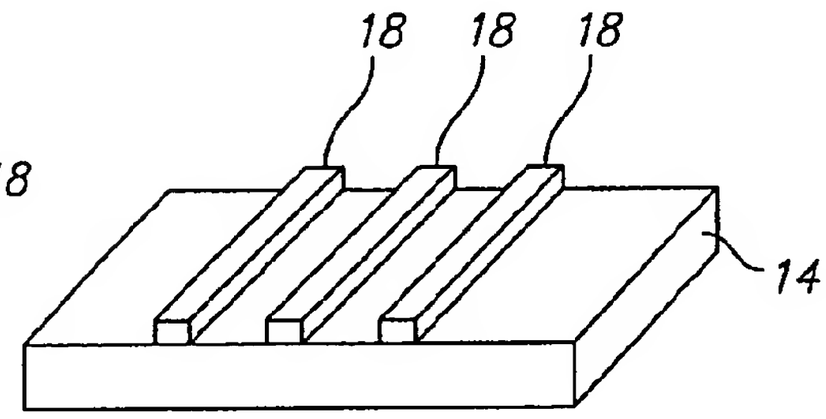



FIG.3b
PRIOR ART

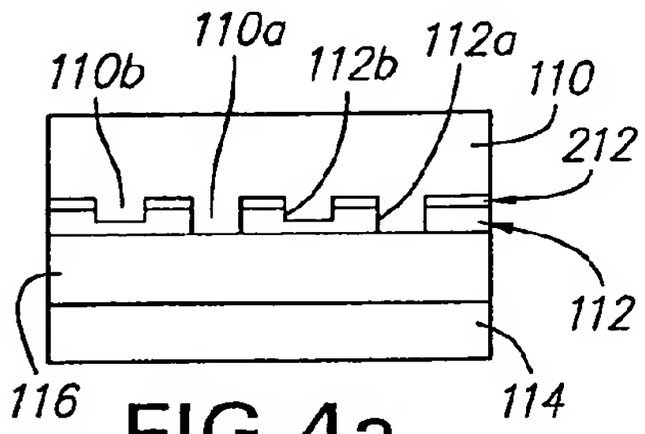



FIG.4a

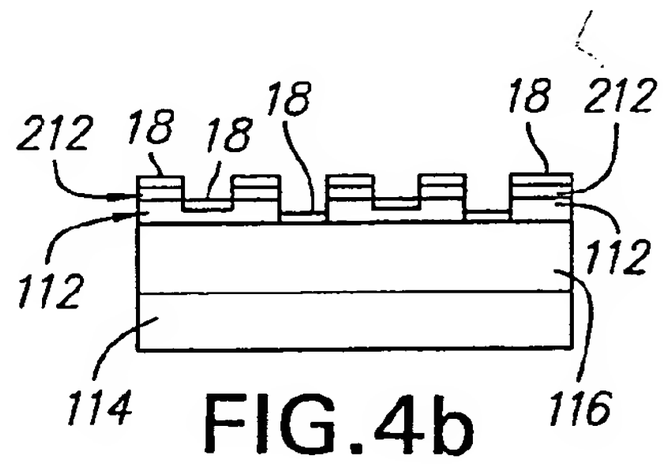



FIG.4b

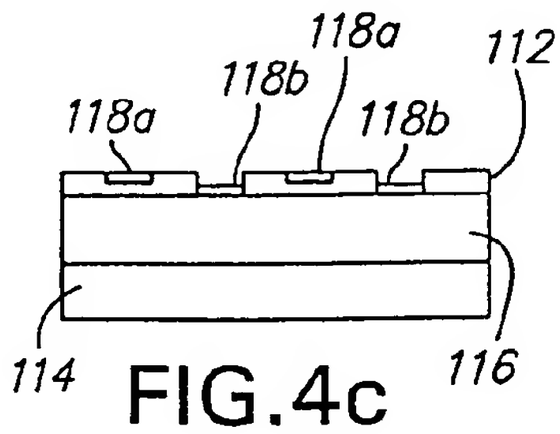



FIG.4c

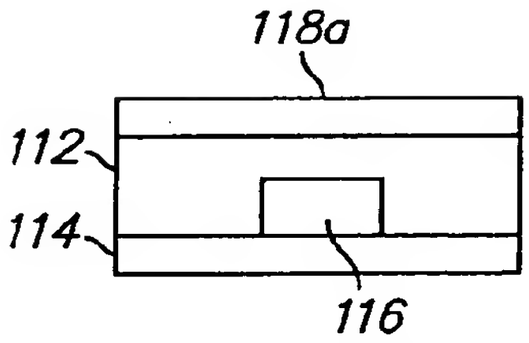



FIG.5a

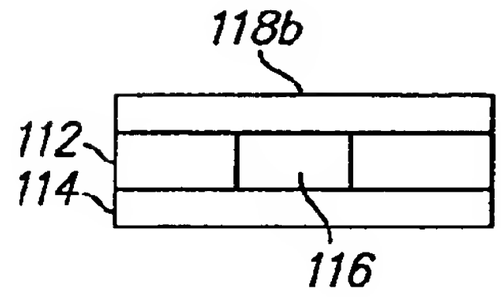



FIG.5b

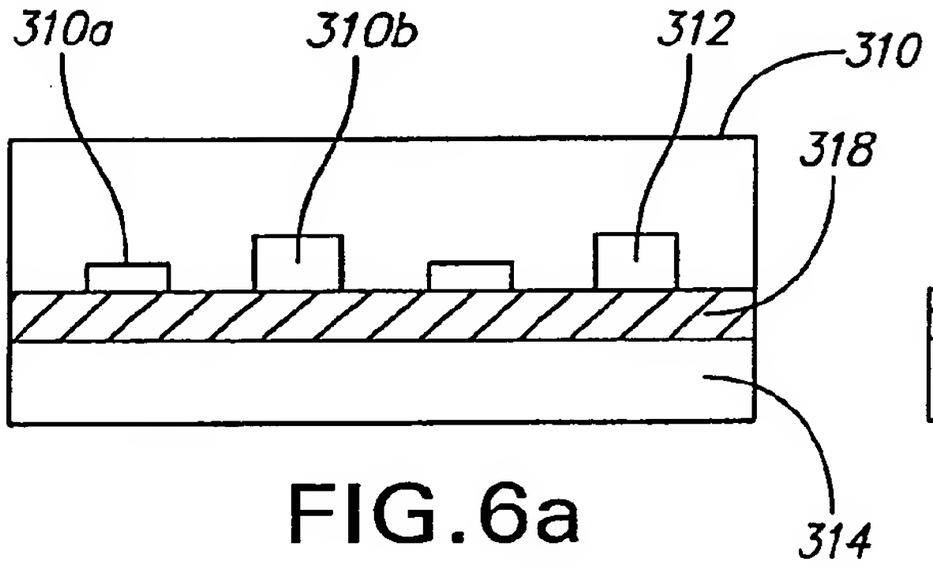



FIG.6a

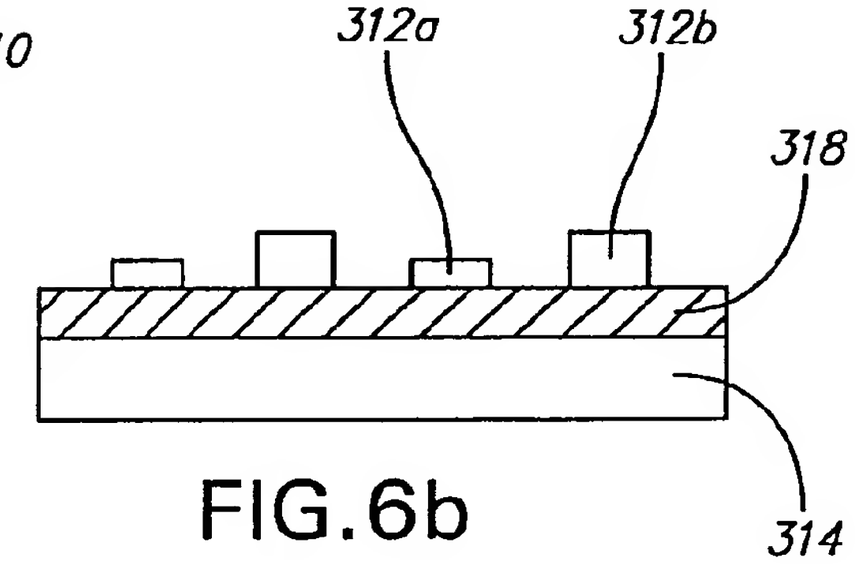



FIG.6b

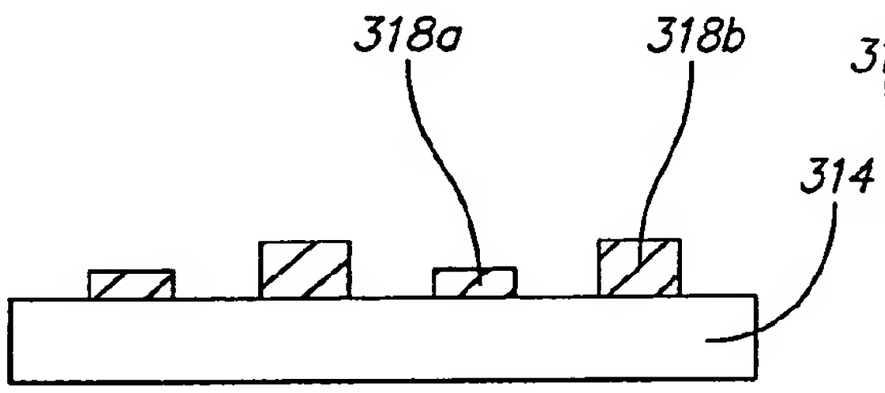



FIG.6c

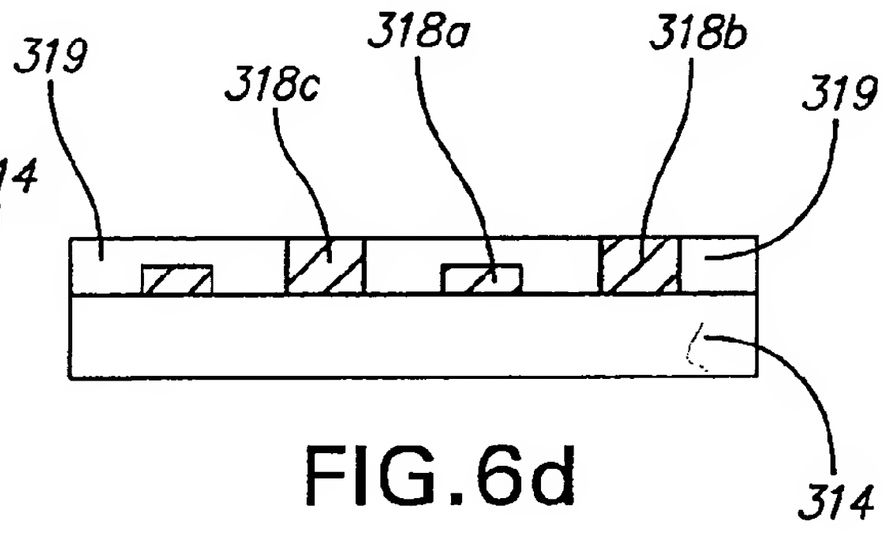



FIG.6d

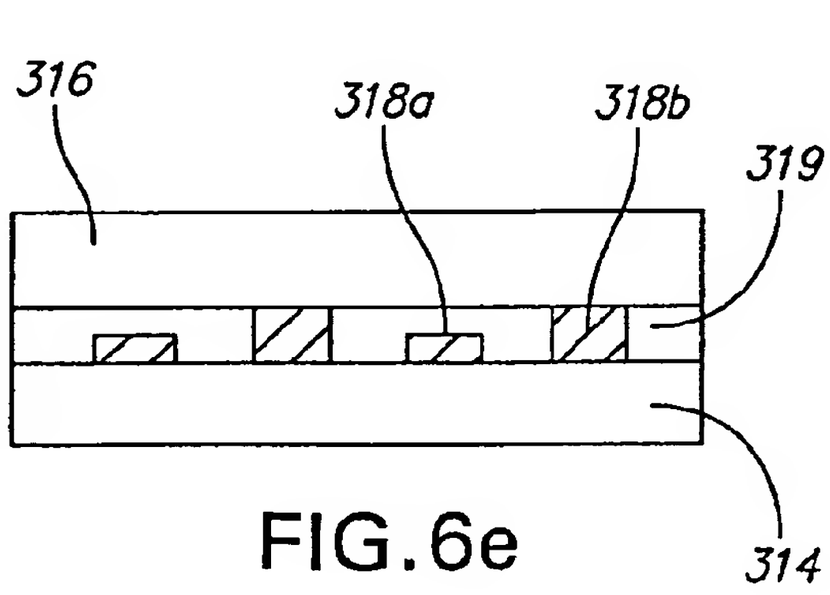



FIG.6e

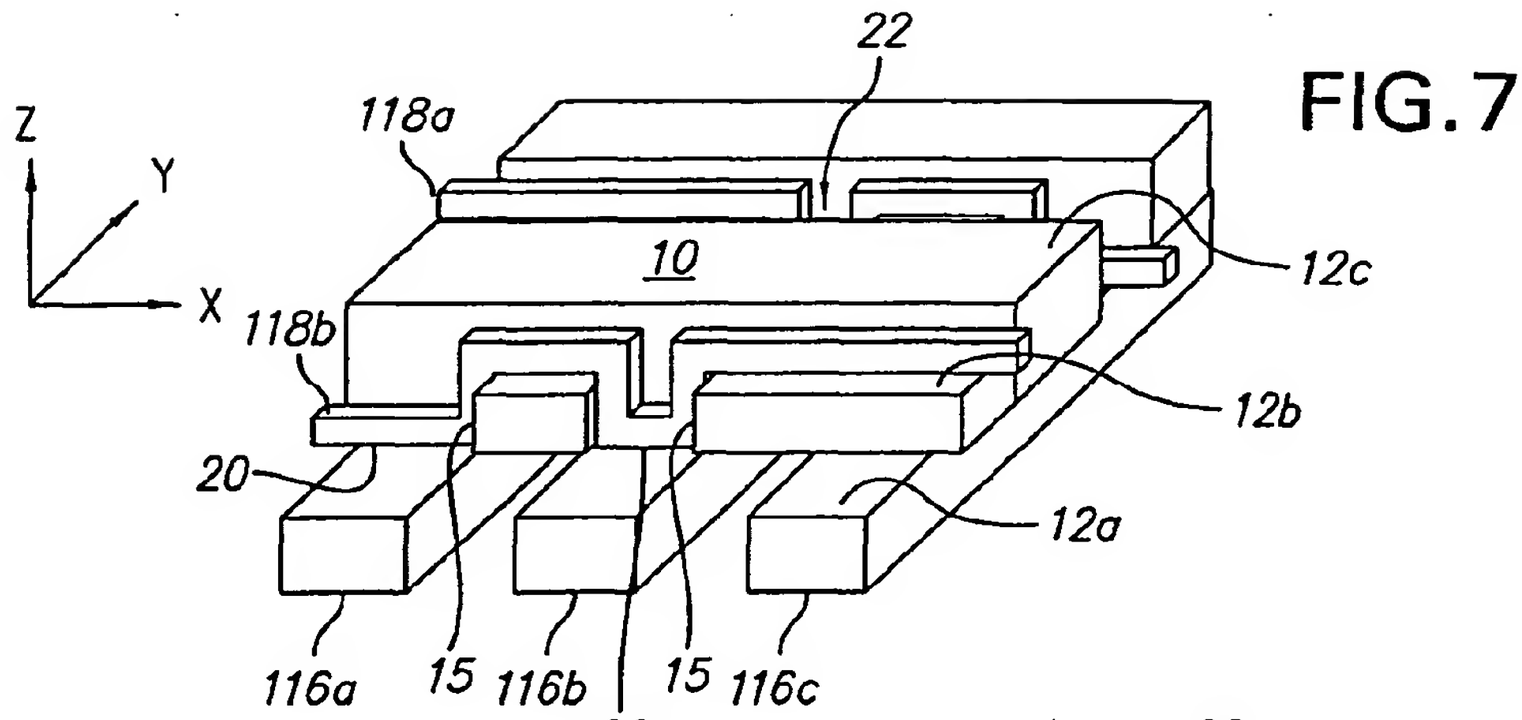



FIG.7

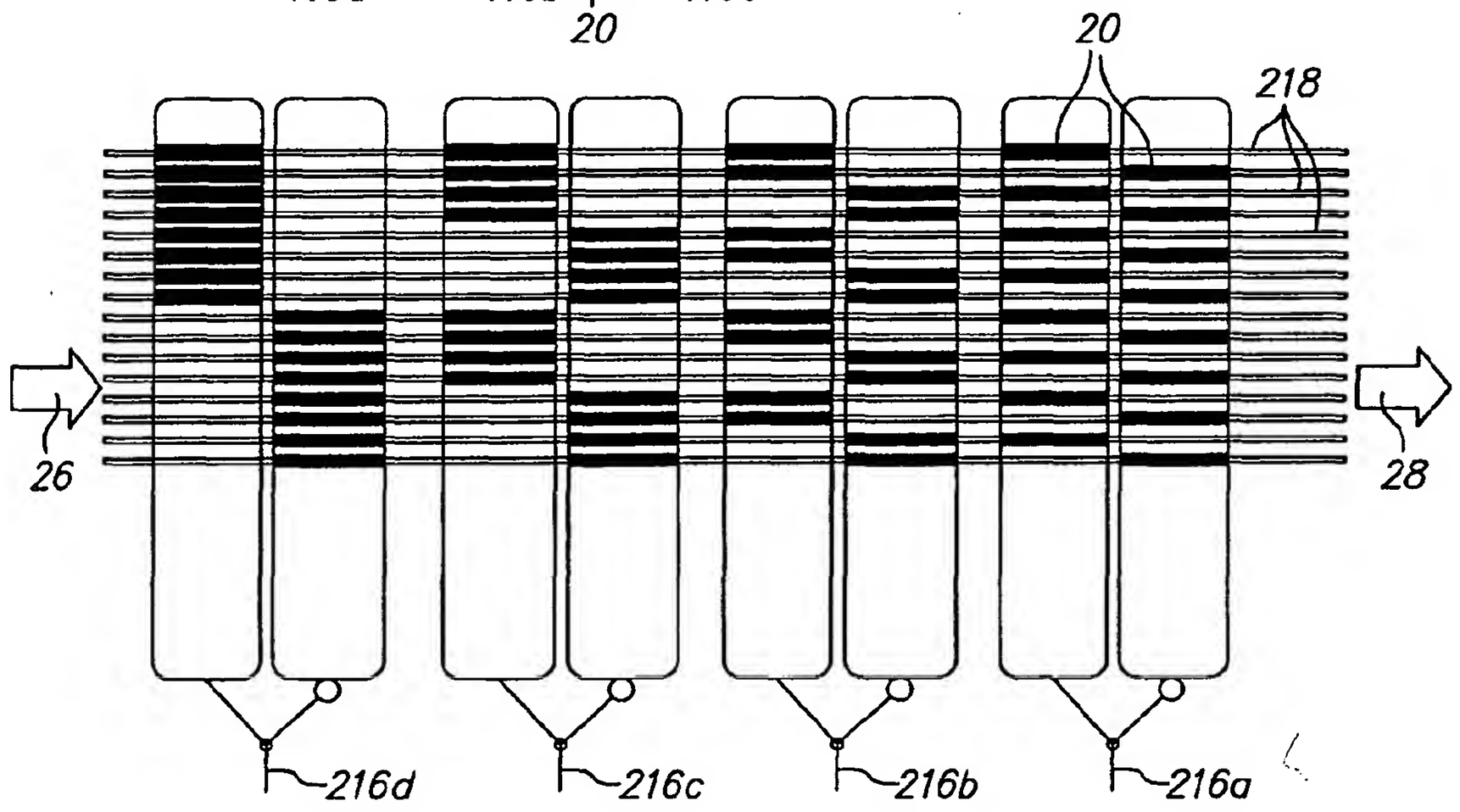



FIG.8

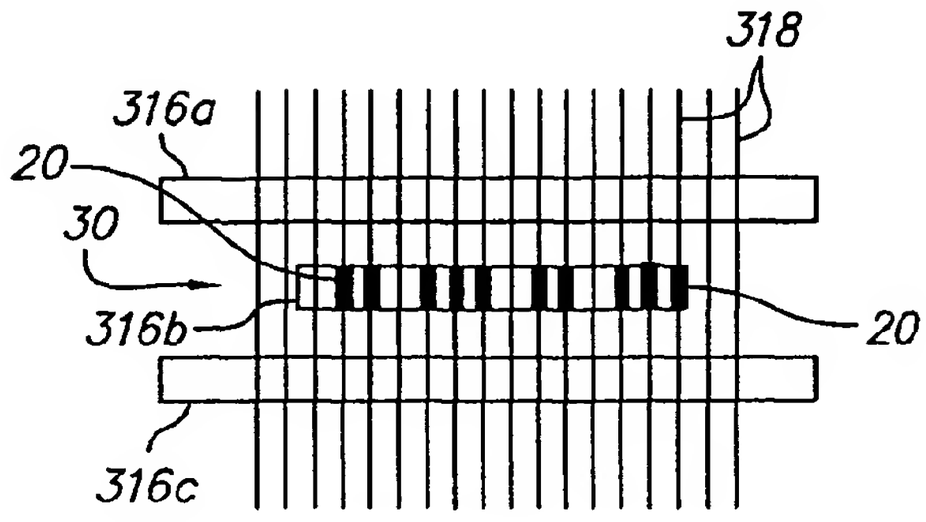
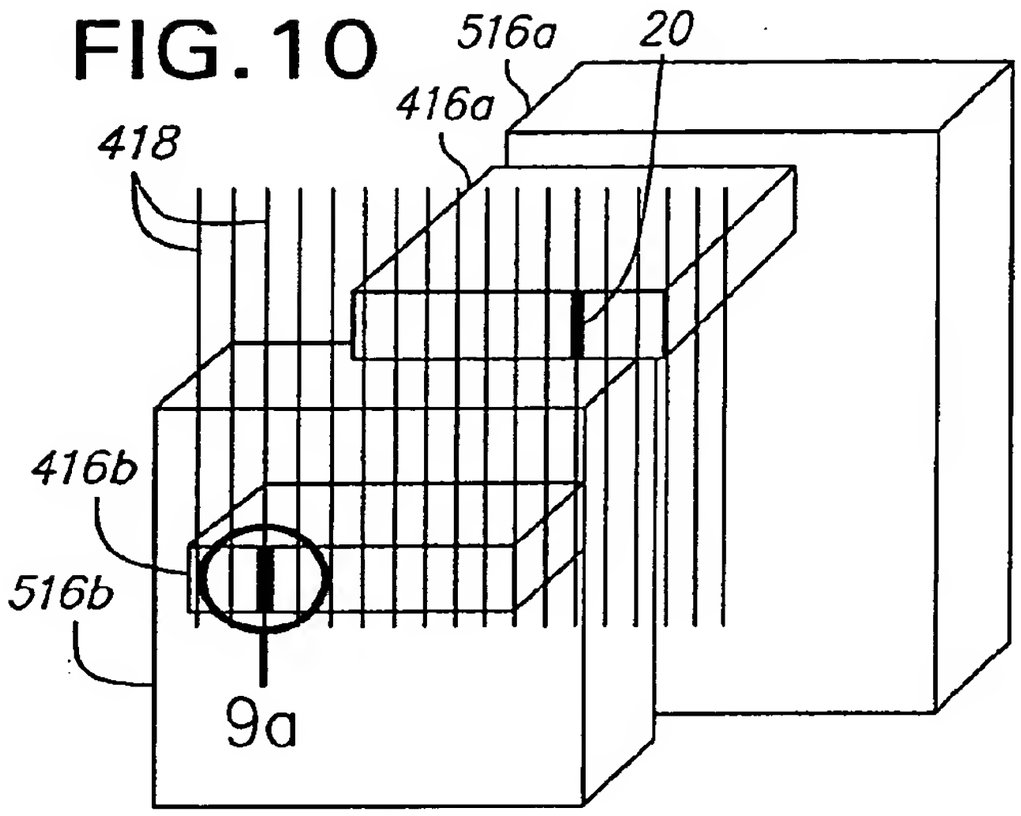



FIG.9

FIG.10



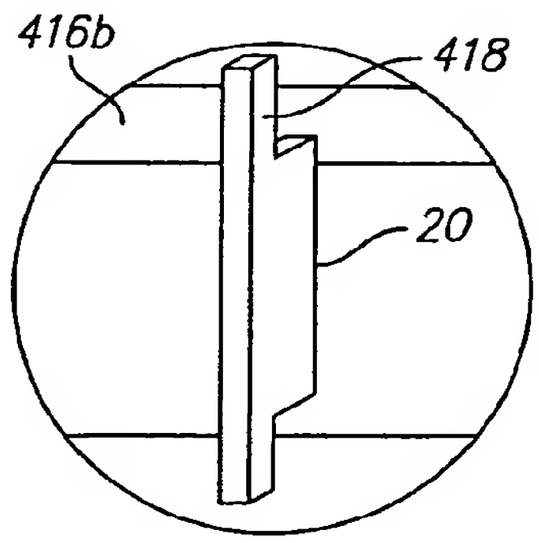




FIG.10a

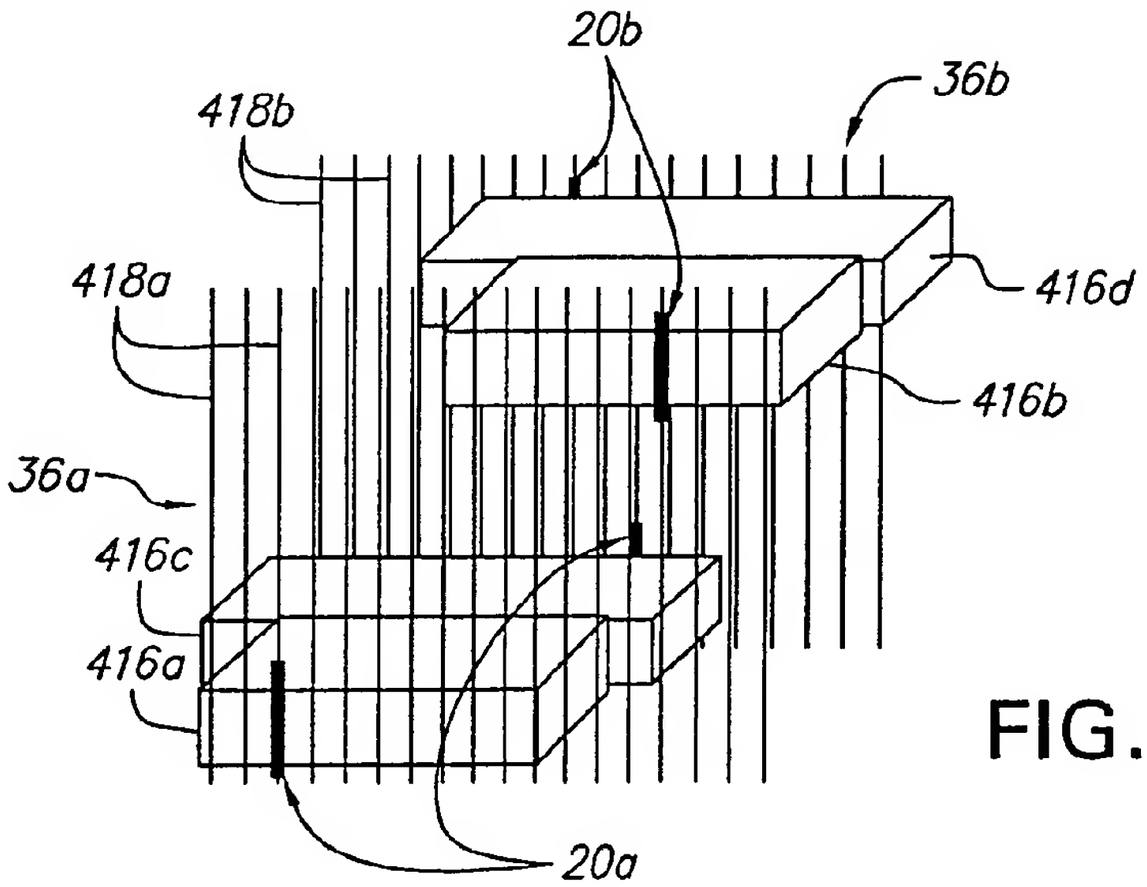



FIG.11

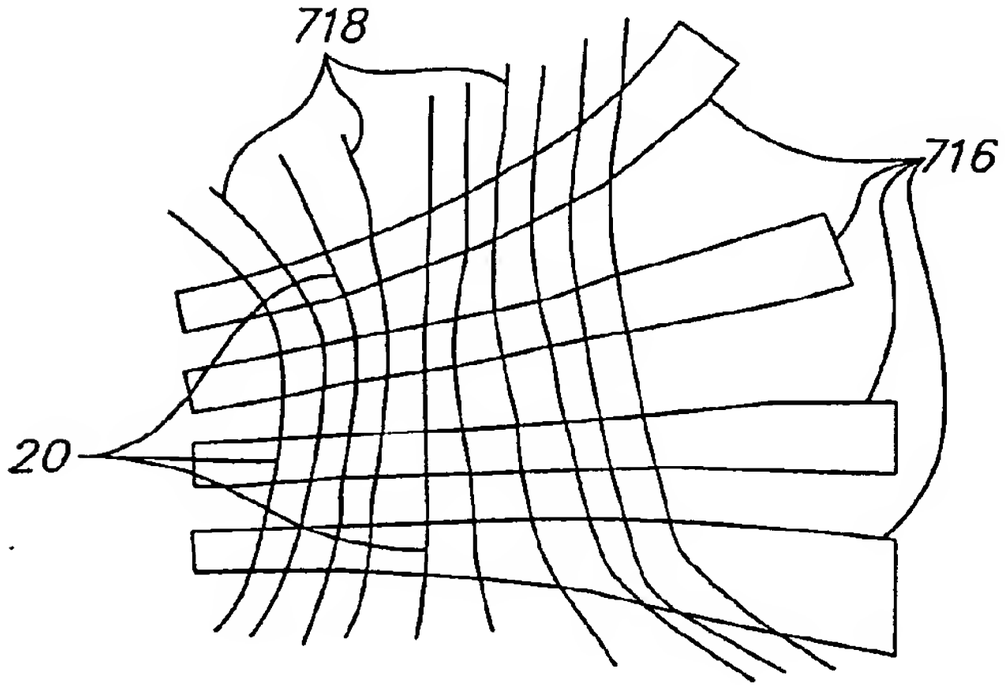



FIG.13

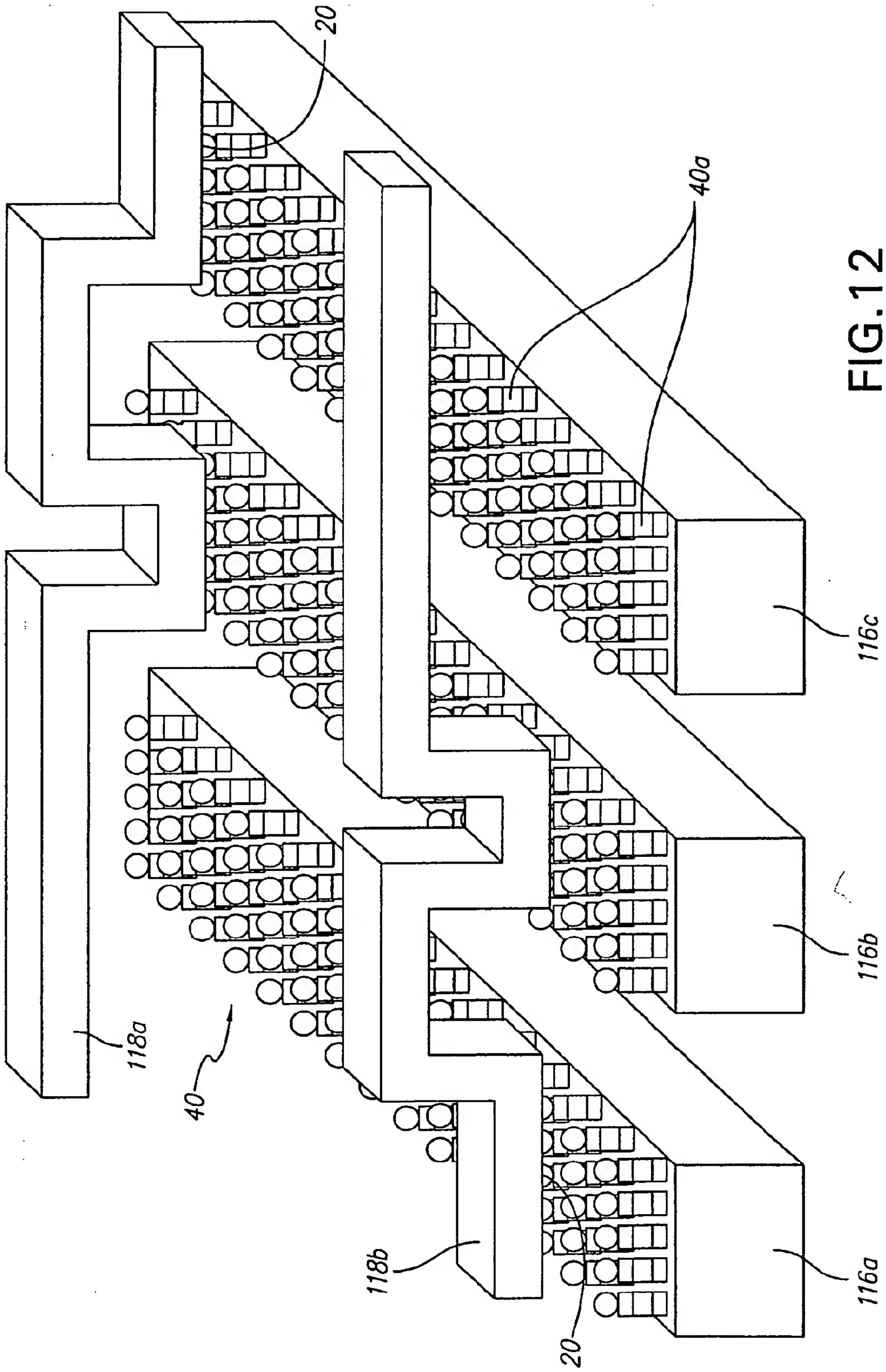



FIG.12

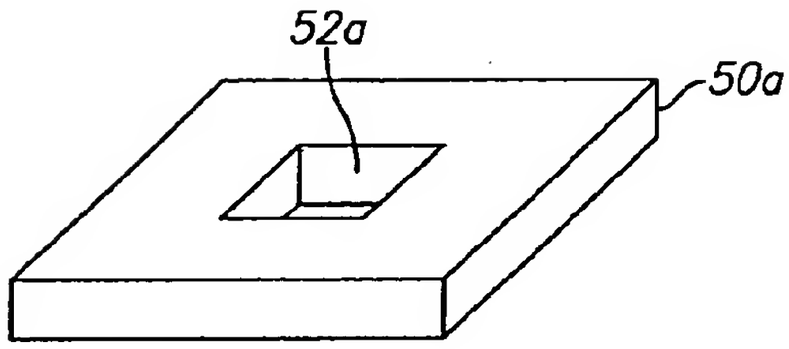



FIG.14a

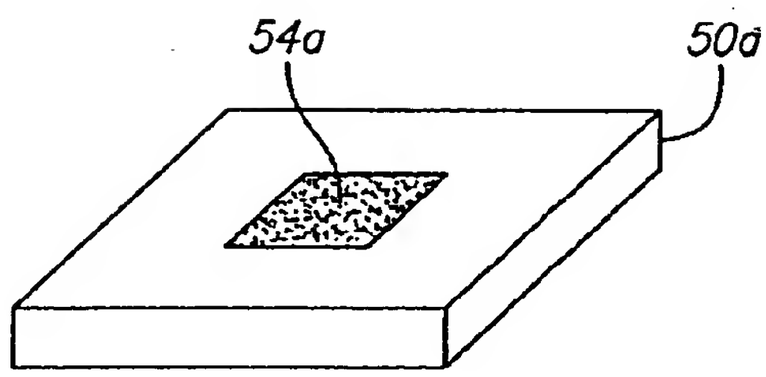



FIG.14b

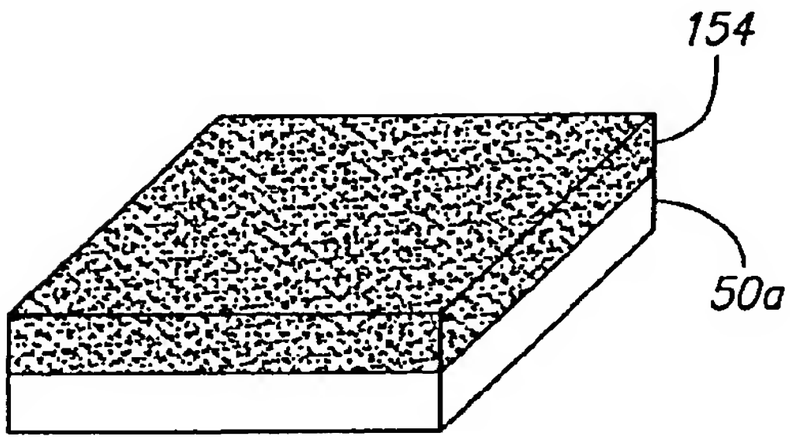



FIG.14c

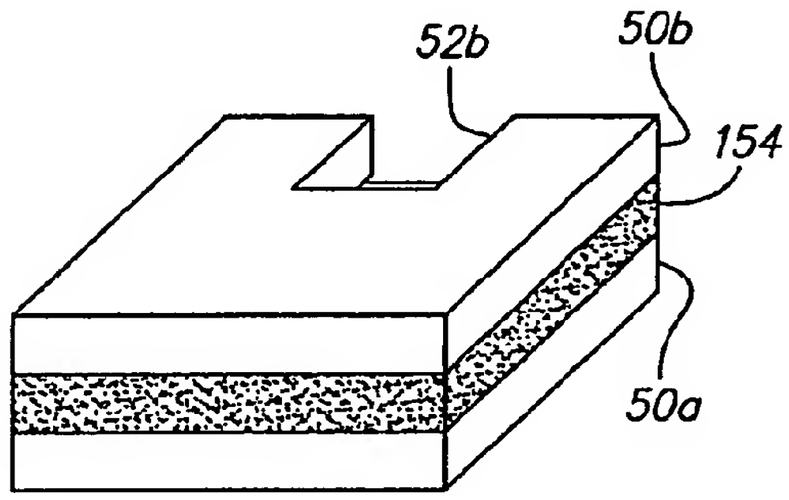



FIG.14d

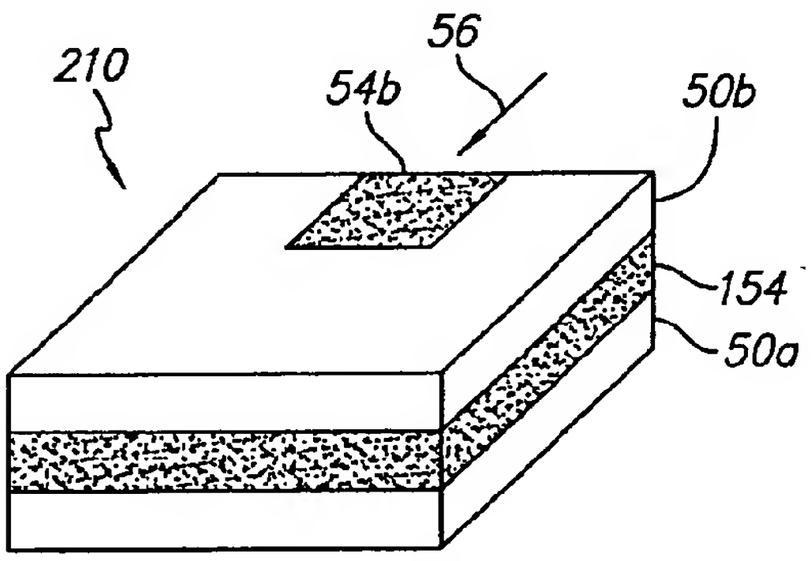



FIG.14e

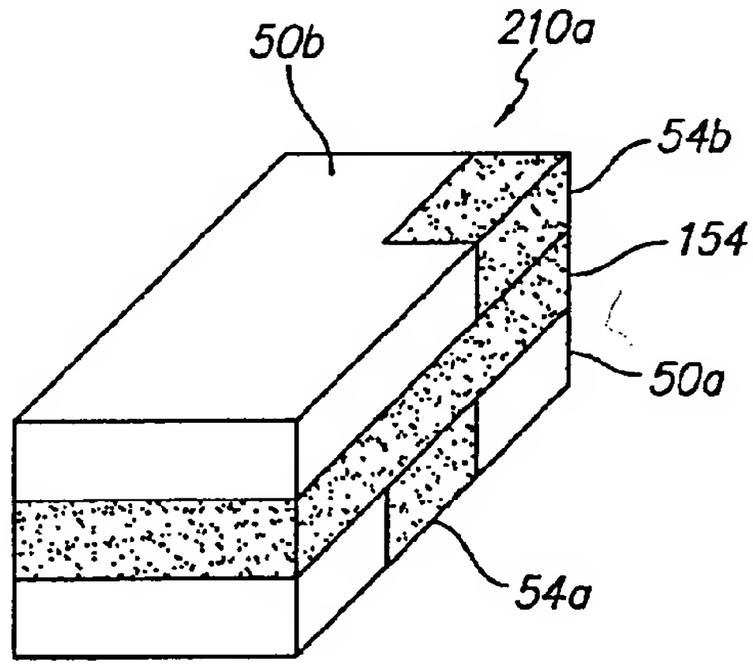



FIG.14f

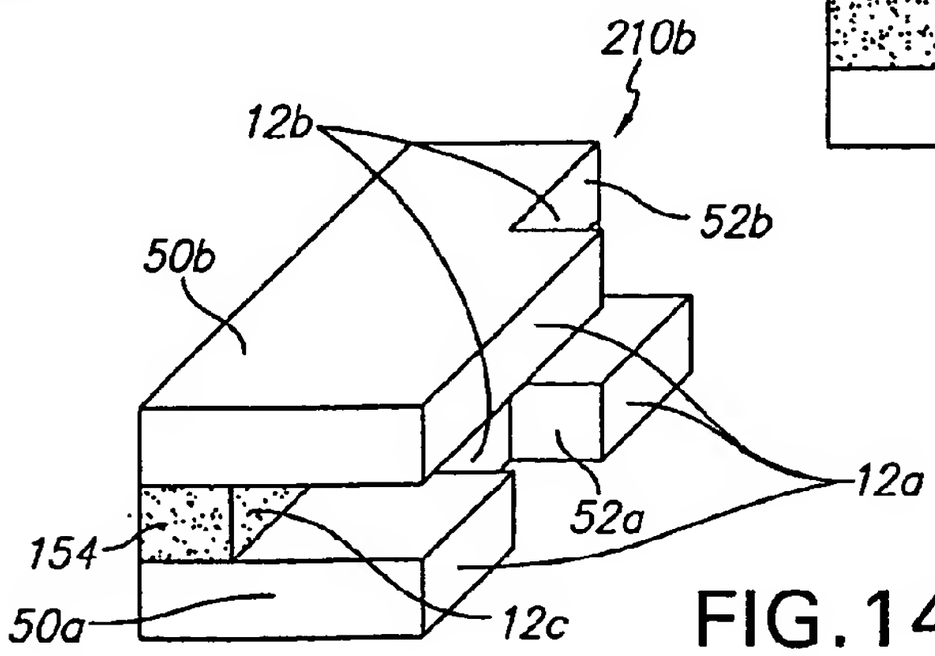



FIG.14g

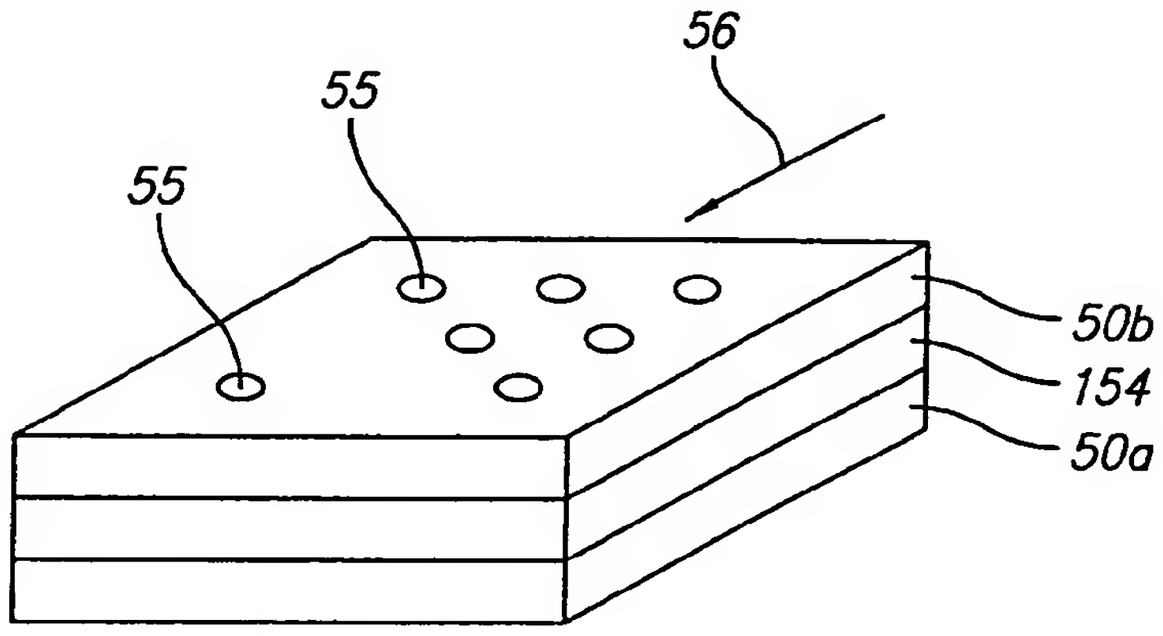



FIG.15a

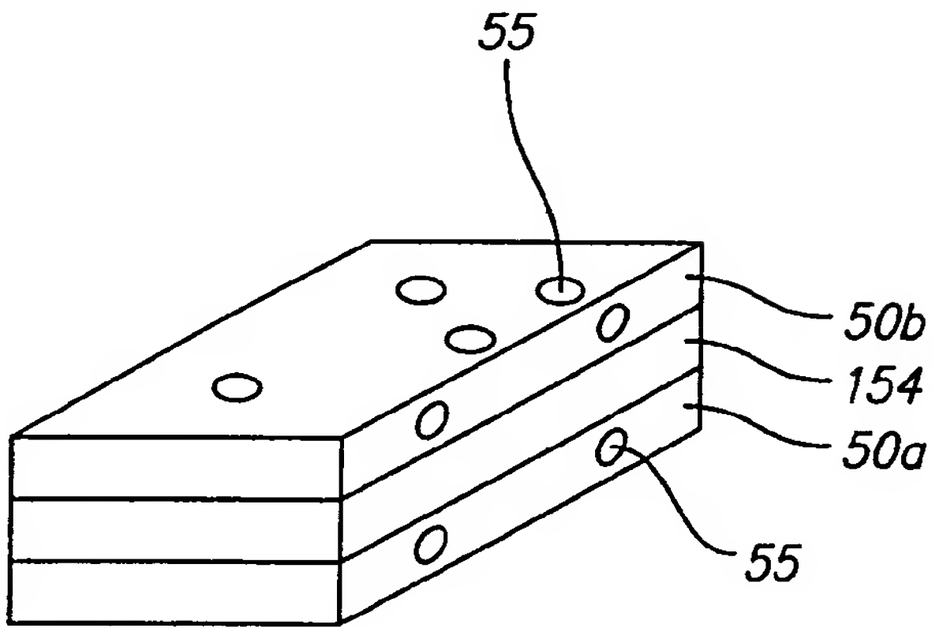



FIG.15b

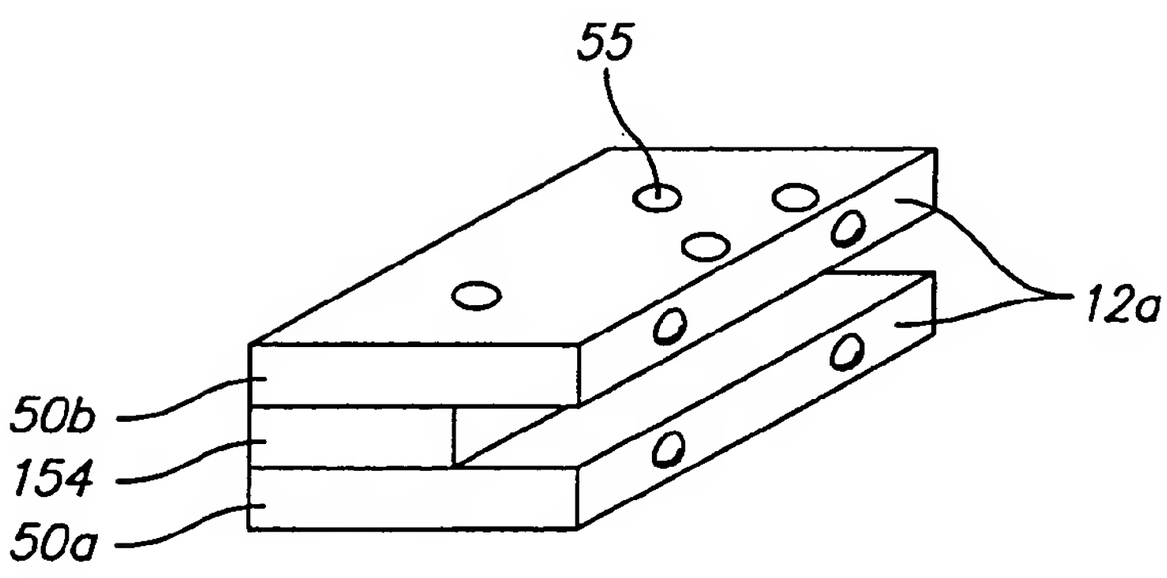



FIG.15c